CBCS SCHEME

USN | | | | | | | | | | |

18EE35

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Write the truth table of the logic circuit having and inputs a, b and c and an output $y = ab\bar{c} + \bar{a}bc + abc$. Also simplify the Boolean expression and implement the logic circuit using NAND gates only. **(06 Marks)**

b. Minimize the following multiple output functions using K-map
i) $f_1(a, b, c, d) = \Sigma m(1, 5, 7, 8, 9, 10, 11, 13, 15)$
ii) $f_2(a, b, c, d) = \Sigma m(1, 2, 6, 7\ 8, 13, 14, 15) + \Sigma d(3, 5, 12)$. **(10 Marks)**

c. Define Canonical Minterm form and canonical Maxterm form. **(04 Marks)**

OR

2 a. Convert the following Boolean function into their proper canonical form in decimal notation.
i) $f = \bar{a}b + bc$ ii) $f = (\bar{x} + y)(y + \bar{z})$. **(08 Marks)**

b. Simplify using Quine-Mccluskey minimization technique for the following function.
$f(w, x, y, z) = \Sigma(0, 1, 4, 5, 9, 11, 13, 15)$. **(12 Marks)**

Module-2

3 a. Design a combinational circuit that will multiply two 2-bit numbers. **(12 Marks)**

b. Implement full subtractor using 3 : 8 line decoder with active high outputs and active low enable input. **(08 Marks)**

OR

4 a. Implement the following using 8 to 1 MUX with a, b, c as select lines
$f(a, b, c, d) = \Sigma(0, 1, 5, 6, 7, 9, 10, 15)$ **(08 Marks)**

b. Implement a 1-bit comparator using 2 : 4 decoder 74139. **(04 Marks)**

c. Design a priority encoder for a system with three inputs, with the middle bit with highest priority encoding to 10, the MSB with the next priority encoding to 11, while the LSB with the least priority encoding to 01. **(08 Marks)**

Module-3

5 a. With a neat diagram, explain the working of master–slave JK flip-flop along with waveforms. **(10 Marks)**

b. Explain switch debouncer using SR latch with waveforms. **(10 Marks)**

OR

6 a. Write the characteristic equation of SR, JK, D and T flip-flops. **(08 Marks)**

b. Differentiate sequential logic circuit and combinational logic circuit. **(04 Marks)**

c. Explain the operation of SR latch with an example. **(08 Marks)**

Module-4

7 a. Design a 4-bit register using positive edge triggered D-flip-flop to operate as indicated in the table below : **(12 Marks)**

Mode select		Data line selected	Register operation
a_1	a_0		
0	0	d_0	Hold
0	1	d_1	Shift right
1	0	d_2	Shift left
1	1	d_3	Parallel load

b. Design a 4-bit mod-8 Johnson counter and also write the count sequence table. **(08 Marks)**

OR

8 a. Design a 4-bit binary ripple up counter using positive edge triggered t-flip-flop with a count enable line. Write the counting sequence and relevant timing diagram. **(08 Marks)**

b. Design a synchronous counter to count the sequence 0, 1, 4, 6, 7, 5 and repeat using positive edge triggered JK flip-flops. **(12 Marks)**

Module-5

9 a. Explain Mealy and Moore model in a sequential circuit analysis. **(08 Marks)**

b. Design a sequential circuit using D-flip-flop for the state diagram. Show below in Fig.Q9(b). **(12 Marks)**

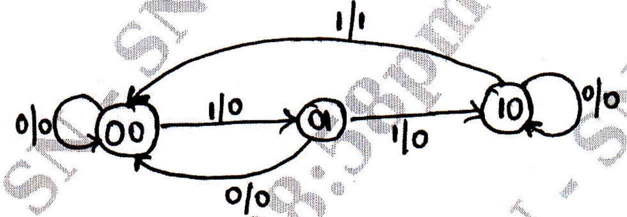

Fig.Q9(b)

OR

10 a. Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit shown in Fig.Q10(a). **(12 Marks)**

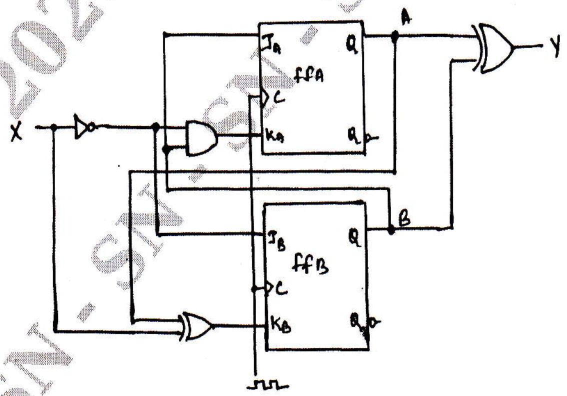

Fig.Q10(a)

b. Write short notes on :
i) ROM ii) RAM iii) EPROM iv) Flash Memory. **(08 Marks)**

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